CLAIMS

What is claimed is:

1. A digital baseband (DBB) receiver for adjusting the frequency domain response of at least one of the real and imaginary signal components of a wireless communication signal, the DBB receiver comprising:

(a) a demodulator having real and imaginary signal outputs, the demodulator for receiving the communication signal and outputting real and imaginary signal components of the communication signal on the real and imaginary signal outputs;

(b) a digital high pass filter compensation (HPFC) module having real and imaginary signal paths;

(c) at least one analog real signal path high pass filter (HPF) in communication with the real signal output of the demodulator and the real signal path of the digital HPFC module; and

(d) at least one analog imaginary signal path HPF in communication with the imaginary signal output of the demodulator and the imaginary signal path of the digital HPFC module, wherein the digital HPFC module suppresses group delay variation distortion caused by at least one of the analog real and imaginary HPFs.

2. The DBB receiver of claim 1 wherein the digital HPFC module comprises:

(i) a real signal input for receiving the real signal component;

(ii) a real compensated signal output for outputting a real compensated output signal;

(iii) a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(iv) a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital

HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(v) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(vi) a sample delay unit having an input and an output, the input of the sample delay unit being connected to the output of the second adder;

(vii) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(viii) a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module.

3. The DBB receiver of claim 2 wherein a cutoff frequency, established by the analog real signal path HPF for the real signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

4. The DBB receiver of claim 2 wherein the gain of the high pass response of the real signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

5. The DBB receiver of claim 2 wherein the output of the second multiplier is subtracted from the real signal component via the third adder.

6. The DBB receiver of claim 2 wherein the output of the sample delay unit is subtracted from the real signal component via the first adder.

7. The DBB receiver of claim 1 wherein the digital HPFC module comprises:

(i) an imaginary signal input for receiving the imaginary signal component;

(ii) an imaginary compensated signal output for outputting an imaginary compensated output signal;

(iii) a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(iv) a first adder having first and second inputs and an output, the first input of the first adder being connected to the imaginary signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(v) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(vi) a sample delay unit having an input and an output, the input of the sample delay unit being connected to the output of the second adder;

(vii) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(viii) a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the imaginary compensated signal output of the digital HPFC module.

8. The DBB receiver of claim 7 wherein a cutoff frequency, established by the analog imaginary signal path HPF for the imaginary signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

9. The DBB receiver of claim 7 wherein the gain of the high pass response of the imaginary signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

10. The DBB receiver of claim 7 wherein the output of the second multiplier is subtracted from the imaginary signal component via the third adder.

11. The DBB receiver of claim 7 wherein the output of the sample delay unit is subtracted from the imaginary signal component via the first adder.

12. The DBB receiver of claim 1 wherein the digital HPFC module is selectively enabled or disabled.

13. A wireless transmit/receive unit (WTRU) for adjusting the frequency domain response of at least one of the real and imaginary signal components of a wireless communication signal, the WTRU comprising:

(a) a demodulator having real and imaginary signal outputs, the demodulator for receiving the communication signal and outputting real and imaginary signal components of the communication signal on the real and imaginary signal outputs;

(b) a digital high pass filter compensation (HPFC) module having real and imaginary signal paths;

(c) at least one analog real signal path high pass filter (HPF) in communication with the real signal output of the demodulator and the real signal path of the digital HPFC module; and

(d) at least one analog imaginary signal path HPF in communication with the imaginary signal output of the demodulator and the imaginary signal path of the digital HPFC module, wherein the digital HPFC module suppresses group delay variation distortion caused by at least one of the analog real and imaginary HPFs.

14. The WTRU of claim 13 wherein the digital HPFC module comprises:

(i) a real signal input for receiving the real signal component;

(ii) a real compensated signal output for outputting a real compensated output signal;

(iii) a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(iv) a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(v) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(vi) a sample delay unit having an input and an output, the input of the sample delay unit being connected to the output of the second adder;

(vii) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(viii) a third adder having first and second inputs and an output, the

first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module.

15. The WTRU of claim 14 wherein a cutoff frequency, established by the analog real signal path HPF for the real signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

16. The WTRU of claim 14 wherein the gain of the high pass response of the real signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

17. The WTRU of claim 14 wherein the output of the second multiplier is subtracted from the real signal component via the third adder.

18. The WTRU of claim 14 wherein the output of the sample delay unit is subtracted from the real signal component via the first adder.

19. The WTRU of claim 13 wherein the digital HPFC module comprises:

(i) an imaginary signal input for receiving the imaginary signal component;

(ii) an imaginary compensated signal output for outputting an imaginary compensated output signal;

(iii) a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(iv) a first adder having first and second inputs and an output, the

first input of the first adder being connected to the imaginary signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(v) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(vi) a sample delay unit having an input and an output, the input of the sample delay unit being connected to the output of the second adder;

(vii) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(viii) a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the imaginary compensated signal output of the digital HPFC module.

20. The WTRU of claim 19 wherein a cutoff frequency, established by the analog imaginary signal path HPF for the imaginary signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

21. The WTRU of claim 19 wherein the gain of the high pass response of the imaginary signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

22. The WTRU of claim 19 wherein the output of the second multiplier is subtracted from the imaginary signal component via the third adder.

23. The WTRU of claim 19 wherein the output of the sample delay unit is subtracted from the imaginary signal component via the first adder.

24. The WTRU of claim 13 wherein the digital HPFC module is selectively enabled or disabled.

25. An integrated circuit (IC) for adjusting the frequency domain response of at least one of the real and imaginary signal components of a wireless communication signal, the IC comprising:

(a) a demodulator having real and imaginary signal outputs, the demodulator for receiving the communication signal and outputting real and imaginary signal components of the communication signal on the real and imaginary signal outputs;

(b) a digital high pass filter compensation (HPFC) module having real and imaginary signal paths;

(c) at least one analog real signal path high pass filter (HPF) in communication with the real signal output of the demodulator and the real signal path of the digital HPFC module; and

(d) at least one analog imaginary signal path HPF in communication with the imaginary signal output of the demodulator and the imaginary signal output of the digital HPFC module, wherein the digital HPFC module suppresses group delay variation distortion caused by at least one of the analog real and imaginary HPFs.

26. The IC of claim 25 wherein the digital HPFC module comprises:

(i) a real signal input for receiving the real signal component;

(ii) a real compensated signal output for outputting a real compensated output signal;

(iii) a first multiplier having first and second inputs and an output,

the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(iv) a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(v) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(vi) a sample delay unit having an input and an output, the input of the sample delay unit being connected to the output of the second adder;

(vii) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(viii) a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module.

27. The IC of claim 26 wherein a cutoff frequency, established by the analog real signal path HPF for the real signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

28. The IC of claim 26 wherein the gain of the high pass response of the real signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

29. The IC of claim 26 wherein the output of the second multiplier is subtracted from the real signal component via the third adder.

30. The IC of claim 26 wherein the output of the sample delay unit is subtracted from the real signal component via the first adder.

31. The IC of claim 25 wherein the digital HPFC module comprises:

(i) an imaginary signal input for receiving the imaginary signal component;

(ii) an imaginary compensated signal output for outputting an imaginary compensated output signal;

(iii) a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(iv) a first adder having first and second inputs and an output, the first input of the first adder being connected to the imaginary signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(v) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(vi) a sample delay unit having an input and an output, the input of the sample delay unit being connected to the output of the second adder;

(vii) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(viii) a third adder having first and second inputs and an output, the

first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the imaginary compensated signal output of the digital HPFC module.

32. The IC of claim 31 wherein a cutoff frequency, established by the analog imaginary signal path HPF for the imaginary signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

33. The IC of claim 31 wherein the gain of the high pass response of the imaginary signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

34. The IC of claim 31 wherein the output of the second multiplier is subtracted from the imaginary signal component via the third adder.

35. The IC of claim 31 wherein the output of the sample delay unit is subtracted from the imaginary signal component via the first adder.

36. The IC of claim 25 wherein the digital HPFC module is selectively enabled or disabled.